



TEKLAB Breadboard IC Trainer Kit is designed to fulfil need of doing experiments of Analog Electronics in Single Trainer. This makes it easy to design, experiment with, and test circuitry without etching and soldering PCB. Students explore a wide variety of electronic concepts simply by sticking components into the Bread Board. All connections and controls are clearly marked and conveniently located.

It is very useful in Analog Electronics laboratories for performing experiments in colleges and universities. It is also useful in testing and making projects related to electronics.

TECHNICAL SPECIFICATIONS

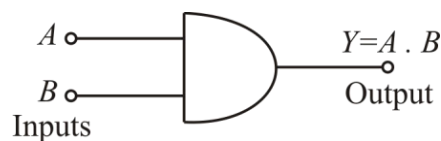
Supply Voltage	230V AC, ±10%, 50Hz
Terminal	2mm BT-5 Terminal
Output Voltage of Trainer	+ 5V / 1A, ±12V / 500mA
Clock	1Hz, 10Hz, 100Hz, 1KHz, 10KHz and 100KHz and 1MHz
Display	2 Nos. 7-Segments Display (BCD to Decimal)
Logic Input	12 Nos. Toggle Input Switch (Logic High & Logic Low)
Logic Output	12 Nos. High Bright RED LED's.
Monopulser	01 High and 01 Low.
Bread Board	840 Tie Point Import Qualities. (Two)

**All specifications and appearances are subject to change without prior notice.*

TRUTH TABLE VERIFICATION OF GATES

01. AND GATE (IC 7408)

A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

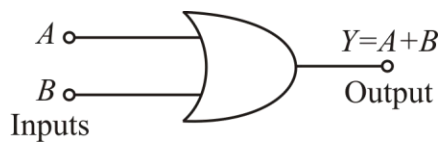


To verify the truth table of AND Gate

1. Insert the IC in the ZIF Socket and lock it.
2. Connect VCC to 5V and Ground Terminal as shown in the pin detail.
3. Connect the input pins A and B to toggle switches.
4. Connect the output terminal Y to the LED point.
5. By setting different values for A and B using toggle switch observe the output on the LED corresponding value of Y in the truth table.

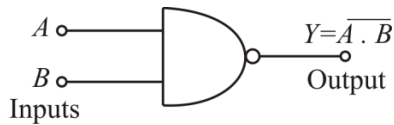
02. OR GATE (IC 7432)

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1



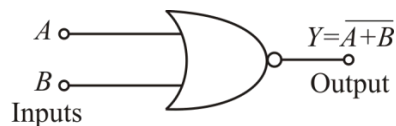
03. NAND GATE (IC 7400)

INPUTS		AND	OUTPUTS
A	B	$A \cdot B$	$Y = \overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



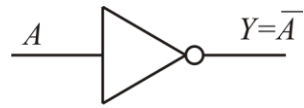
04. NOR GATE (IC 7402)

INPUTS		AND	OUTPUTS
A	B	$A + B$	$Y = \overline{A + B}$
0	0	0	1
0	1	1	1
1	0	1	1
1	1	1	0



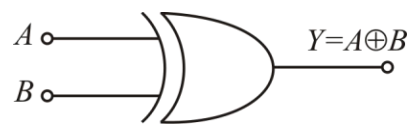
05. NOT GATE (IC 7404)

Input Variable		Output
A		$Y = \bar{A}$
0		1
1		0



06. EX-OR Gate (IC 7486)

A	B	AB	$\bar{A}\bar{B}$	$Y = AB + \bar{A}\bar{B}$ or $A \oplus B$
0	0	0	1	0
0	1	0	0	1
1	0	0	0	1
1	1	1	0	0

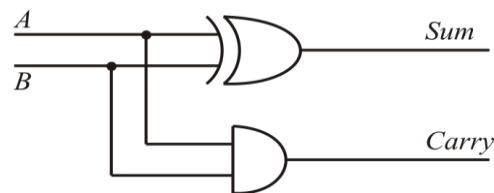


Realization of Half adder using Basic and EX-OR gates.

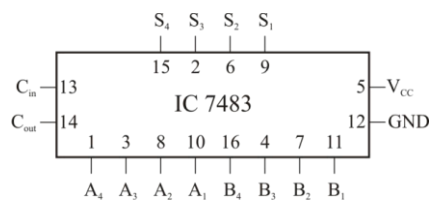
Inputs		Outputs	
A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

IC for EX-OR Gate (IC 7486)

IC for AND Gate (IC7408)



Parallel Adder using 7483 chip



A_1, A_2, A_3, A_4 & B_1, B_2, B_3, B_4 & C_{in} are the inputs

S_1, S_2, S_3, S_4 & C_{out} are the outputs.

Case 1: When $C_{in} = 0$

if	A_4	A_3	A_2	A_1	=	1	1	0	0
	B_4	B_3	B_2	B_1	=	0	0	1	1
Then SUM	S_4	S_3	S_2	S_1	=	1	1	1	1

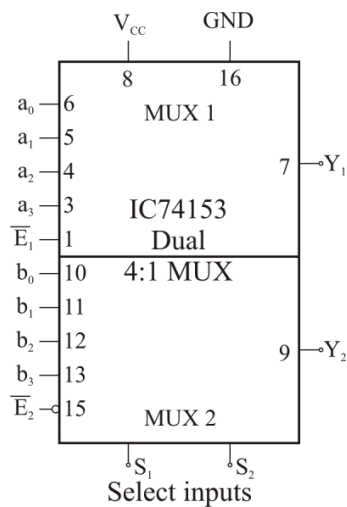
In this case $C_{out} = 0$

Case 2: When $C_{in} = 1$

if	A_4	A_3	A_2	A_1	=	1	0	0	1
	B_4	B_3	B_2	B_1	=	1	1	0	1
Then SUM	S_4	S_3	S_2	S_1	=	0	1	1	1

In this case $C_{out} = 1$

Study of 4: 1 MUX / DEMUX



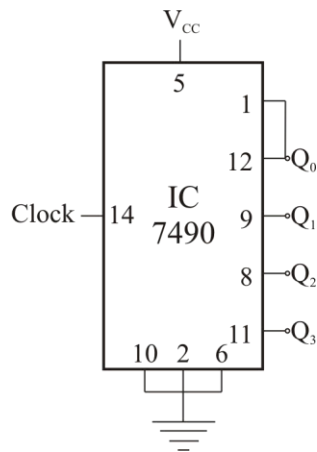
Note:

1. If $E_1 = 0, E_2 = 1$ MUX1 will be selected (Enabled)
2. If $E_1 = 1, E_2 = 0$ MUX2 will be selected (Enabled)
3. If $E_1 = 0, E_2 = 0$ both MUX will be selected (Enabled)
4. If $E_1 = 1, E_2 = 1$ both MUX will be deselected (disabled)

Truth Table of 4: 1 MUX

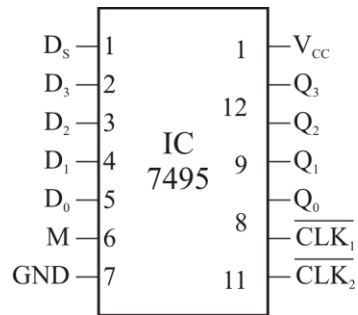
Enable Inputs		Address Select Inputs		Data Input				Output	Comments
\bar{E}_2	\bar{E}_1	S_1	S_0	a_0	a_1	a_2	a_3	Y_1	
1	0	0	0	0	X	X	X	0	a_0 selected
(MUX – 1 Enabled)		0	1	X	0	X	X	0	a_1 selected
		1	0	X	X	0	X	0	a_2 selected
		1	1	X	X	X	0	0	a_3 selected

Counters using 7490 / 7493



Clock Input	Flip Flop Outputs			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

Shift Register using 7495



D_s : Serial input data (to be right shifted)

D_3, D_2, D_1, D_0 : Parallel data inputs.

M= Mode Control

Keep $M = 1$ for loading parallel data and enable clock 2.

$M = 0$ for loading parallel data and enable clock 1.

Q_3, Q_2, Q_1, Q_0 : Parallel outputs of the shift register

Truth-Table for SIPO and SISO

Mode Control	Clock	Pulse	Serial Input Data	Outputs			
				Q_3	Q_2	Q_1	Q_0
0	Clock-1	1	1	1	X	X	X
		2	0	0	1	X	X
		3	1	1	0	1	X
		4	0	0	1	0	1
		5					0
		6					1
		7					0

Parallel Output

Serial Output

Truth-Table for PIPO and PISO

Mode Control	Clock	Parallel Inputs				Pulse	Outputs				
		D ₃	D ₂	D ₁	D ₀		Q ₃	Q ₂	Q ₁	Q ₀	
1	Clk-2	1	0	1	0	1	1	0	1	0	Parallel Output
0	Clk-1					2				1	Serial Output
						3				0	
						4				1	

